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Effects of electrostatic discharge high-field current impulse on oxide breakdown

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Stress testing is performed in two stages, a high-field prestress test followed by an electrostatic discharge (ESD) event, which induces high-field current impulse stress. dc and impulse high-field prestress sources are separately applied to generate different formations of bulk oxide traps, near-interface oxide traps (border traps), and interface traps. Experimental results indicate that the dc prestress testing induces many more interface traps and border traps in the metal-oxide-semiconductor capacitor structure than the impulse prestress testing. Additionally, an anomalous turnaround degradation of oxide breakdown subjected to the following ESD impulse stress is observed and attributed to the effect of border traps. Border traps cannot communicate with interface traps and silicon substrate during high-field current impulse stressing, and therefore cannot emit trapped charges instantaneously. Consequently, these trapped charges provide a negative electric field decreasing the Fowler-Nordheim stress current and therefore reducing the degradation of the oxide breakdown. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2404470]

I. INTRODUCTION

Both bulk and near-interface oxide traps (border traps), as well as the interface traps, are generated during high-field stressing on oxide.[1–3] Since deep-submicron technologies for low-voltage applications reduce the thickness of gate oxide, thinner gate oxide is frailer and easily damaged during electrostatic discharge (ESD). ESD is a form of impulse stress with very high field and current. Immunity to ESD is an important reliability issue in complementary metal-oxide-semiconductor (CMOS) integrated circuits.[4] Latent damage effects induced by ESD on oxide have been widely studied.[5–11] For example, ESD latent damage has been revealed to degrade gate oxide reliability during stressing of hot electron injection. The ESD events degrade the characteristics of CMOS transistors and gate oxide. In addition, the oxide trapped charges are generated by ESD stress and are polarity dependent on different ESD types. However, very few publications have considered the impact of prestress-induced trapped charges in oxides on ESD immunity and performance, although a large knowledge base exists for oxide degradation subjected to high frequency and impulse stress events, such as ESD events.[12–17]

Most electrostatic discharges are present during the processes of forming integrated circuits on wafers or the stage of integrated circuit packaging and handling. As reported in semiconductor manufacturing, widely used plasma processes would stress and degrade the gate oxide integrity of devices due to the exposed nature of the plasma charging environment.[18] The antenna effect current is generally concentrated into the active gate oxide area, resulting in a high current density ranging from 100 mA/cm^2 to 10 A/cm^2. The time duration of charging damage would run from a few seconds to a few tens of seconds, and the total charging time for a fully processed device can be up to 1000 s. Moreover, once plasma arcing occurs, a large transient discharge current with submicrosecond duration would inject itself into gate oxide, leading to severe stress and damage. Except for plasma charging in silicon processing, serial function probing and subsequent burn-in acceleration testing afterward may also impose prestress on the gate oxide of a device.

Transmission line pulsing (TLP) curve tracer test systems can generate serial high-field current impulses and have been widely applied to examine the electrical characteristics of semiconductor device during very short impulse durations and also during the emulation of ESD.[19,20] A TLP tester with 100 ns pulse width and 10 ns rise/fall time can simulate and correlate the performance of human body model (HBM) ESD stress on semiconductor devices. Therefore, TLP can provide strong insight into the electrical characteristics of stress and degradation of gate oxide. This study explores the effect of stress-induced trapped charges on the ESD immunity of oxide for both long durations, as dc, and for very short durations below the microsecond level, as TLP impulse. To investigate different formations of trapped charges induced by dc constant current and TLP impulse current injection, both *I-V* and quasistatic *C-V* characteristics were measured and examined. ESD emulation by TLP was then performed again to evaluate the final oxide degradation and performance. Hence, this study qualitatively characterizes the prestress-induced trapped charges, including bulk oxide trapped charges and border and interface trapped charges, then correlates them with the final oxide characteristics after ESD impulse stress by TLP.

Experimental results reveal that the formations of trapped charges in oxide between dc current prestress and transient TLP impulse current prestress are quite different. dc

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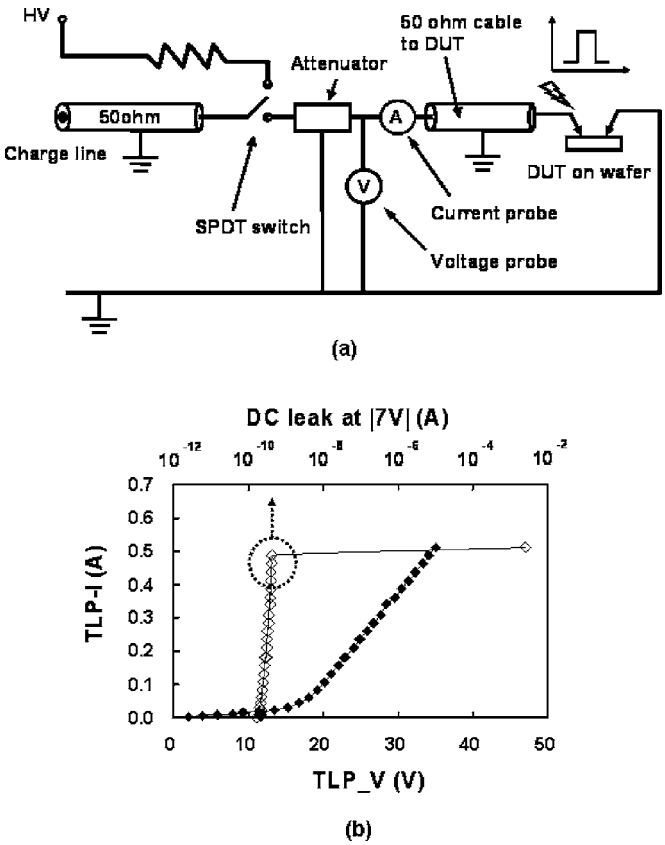

FIG. 1. (a) TLP setup configuration. Square wave forms were applied to a device, while the voltage across and the current through it were measured and the dc leakages between pulses were monitored. (b) TLP measured results of a NMOS capacitor. As shown, device failed as the leakage current exceeded 1 μA.

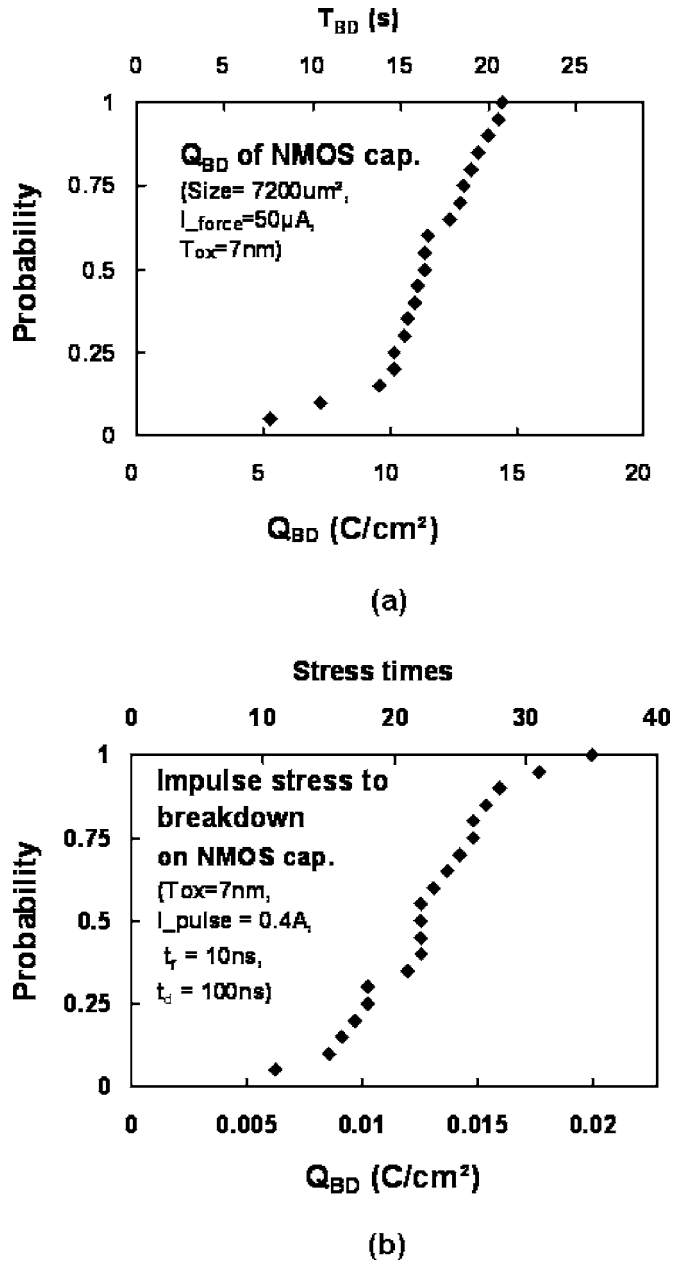

FIG. 2. (a) Distribution of Q_{bd} subjected to dc stress. Typical hard-breakdown field exceeded 13 MV/cm. (b) Distribution of Q_{bd} subjected to 0.4 A TLP impulse stress.

high-field prestress can generate more border and interface traps than TLP impulse prestress. The results of oxide breakdown subjected to ESD impulse stress tests reveal that degradation continues to increase with the increasing periods of TLP impulse prestress. However, the degradation of dc high-field prestress does not continue to increase with the increasing dc prestress time. Significantly, a special turnaround phenomenon occurs, in which the degradation first increases and then decreases as the dc prestress time continues to increase. A possible explanation is given for the observed phenomenon.

II. EXPERIMENT

Experiments were performed on *n*-type MOS (NMOS) capacitors with 7 nm thick gate oxide, fabricated by a standard 0.35 μm CMOS technology. Features of this process included conventional Local Oxidation of Silicon (LOCOS) isolation, twin well, *n*+ polygate with tungsten silicide cap, and tungsten plugged contact. The *I-V* characteristics, quasi-static *C-V* characteristics, and dc constant current stress were all performed with HP 4156C. TLP characteristics were measured by a commercial Barth 4002 pulse curve tracer system. Testers with one contact to the gate and another contact to the substrate were adopted to form the two-probe TLP configuration. The TLP system applied the square wave form with 100 ns pulse width and 10 ns rise/fall time to a device while measuring the voltage across and the current through it. Figure 1(a) illustrates the TLP setup configuration.[19] As the figure shows, the transmission line is a 50 Ω coaxial cable charged by the dc high voltage generator. The settings of start and step voltages of the dc high voltage generator were both 1 V. The discharge voltage was applied and converted into a current pulse by a resistor. The current pulse with a square wave form rises with the voltage provided from the dc high voltage generator. Constant current pulses were then forced into the device, enabling the behavior of devices under high-current conditions to be studied. The robustness on a very short time scale was explored by subjecting the device to incrementally rising voltage pulses and making dc leakage measurements between pulses. Figure 1(b) depicts the measurement results of a NMOS capacitor

with 7 nm of gate oxide. The solid symbols denote the breakdown characteristics measured by increasing current pulses, and the open symbols denote the leakage current measured at |7 V| after each pulse. The gate oxide breakdown measured by TLP was hard. As shown in Fig. 1(b), the leakage at |7 V| (plotted on the top axis versus TLP current) rose by several orders of magnitude exceeding 1 μA (the chosen failure criterion) at this point of breakdown.

All measurements were performed in accumulation. Under quasistatic *C-V* measurement, light was used to generate minority carriers in inversion. Trials were also performed for hold time and step delay time of the voltage steps from 100 ms to a few tens of seconds to ensure similar measurement results under equilibrium condition for all stressed and unstressed samples. dc measurement was performed with a negative bias on the gate of the NMOS capacitor. TLP impulse measurement was conducted with positive bias on the substrate of the NMOS capacitor, since the TLP tester cannot provide negative wave forms. The NMOS capacitors were rectangular in shape and 1200 μm^2 in area. The oxide typical hard breakdown field exceeded 13 MV/cm at the initial check. Figure 2(a) shows the distribution of charge to breakdown (Q_{bd}), where the 50% probability value was 11.39 C/cm^2 and the stress time was 16.4 s under -4.17 A/cm^2 dc current injection. These oxides were of high quality, with the characteristics typically required by modern CMOS fabrication technologies. Figure 2(b) shows the distribution of Q_{bd} subjected to 3.42×10^4 A/cm^2 TLP impulse stress. To avoid screen effect arising from the prestress process, the maximum stress time for the dc prestress was set to 10 s and the maximum number of stress periods for the TLP impulse prestress was set to 12, each at the same current density of cumulative Q_{bd} measurement. Experimental procedures are described as follows. The dc *I-V* and quasistatic *C-V* characteristics were first measured. The NMOS capacitors were then subjected to dc current prestress at -4.17 A/cm^2 (about -15.5 MV/cm) and to TLP current impulse prestress at 3.42×10^4 A/cm^2 (about -44.3 MV/cm), separately. After certain prestresses, dc *I-V* and quasistatic *C-V* were again measured to obtain the oxide degradation for variable stress periods and pulses. Finally, ESD emulation by TLP measurements was performed to obtain the oxide breakdown parameters and characteristics subjected to high-field current impulse stress.

III. RESULTS AND DISCUSSION

This section presents the effect of different prestress-induced trapped charges on gate oxide characteristics subjected to ESD-like impulse stress. The experiment is comprised of two parts. First, the induced trapped charges by dc constant current and TLP impulse current prestresses were analyzed. Corresponding degradation including bulk and border oxide traps, as well as interface traps, were investigated. The ESD performance of gate oxide after prestresses by dc constant current and TLP impulse current was probed. Mechanisms of gate oxide degradation for two-type prestresses and ESD impulse zapping were presented.

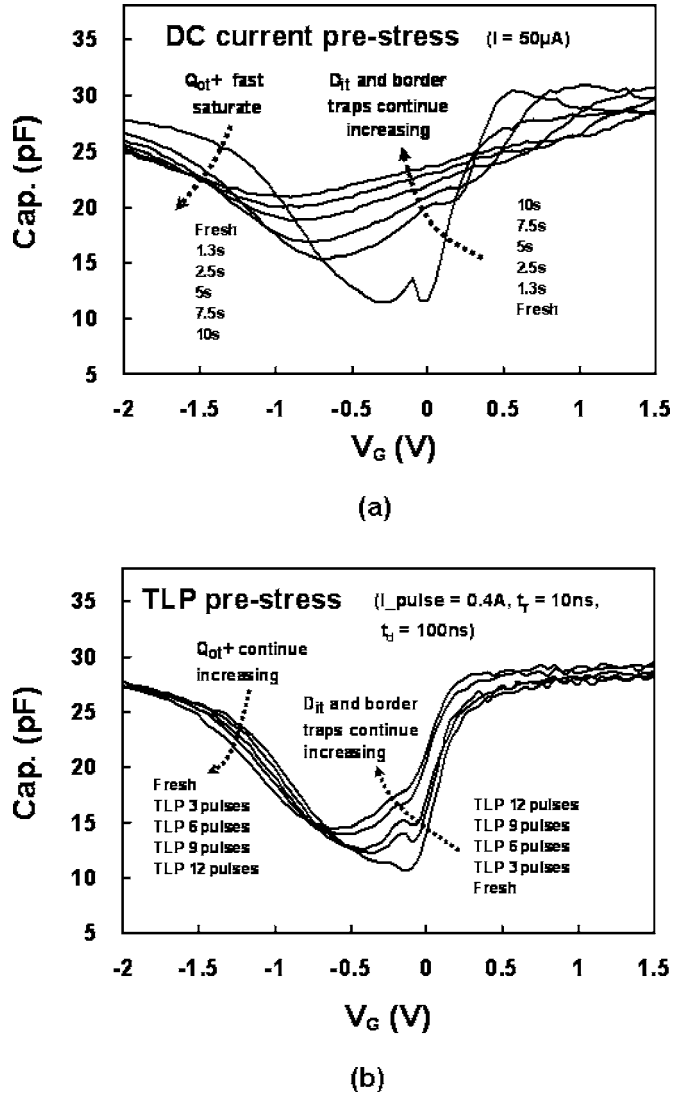

FIG. 3. The quasistatic *C-V* characteristics of NMOS capacitors subjected to (a) dc constant current and (b) TLP impulse current prestress testing. As compared with dc prestress testing, far less interface and border traps were generated by TLP prestress testing.

A. Different formations of traps induced by dc and TLP impulse stress

Both positive and negative oxide trapped charges are generated during current stressing on oxide. Besides the oxide trapped charges, interface trapped charges at the substrate-SiO_2 interface are also generated during the stress.[21,22] Under negative gate stressing, positive oxide trapped charges are close to the substrate interface, while negative oxide trapped charges are close to the gate interface. Hence negative oxide trapped charges have less effect on flatband voltage (FBV) and usually show no obvious effect for FBV shift in *C-V* measurement.[22] A standard viewpoint suggests that the silicon bands bend down under thermal equilibrium conditions when the gate bias was zero. For MOS capacitor with a *p*-type substrate, most donorlike interface traps and some acceptorlike interface traps below the Fermi level were filled, revealing neutral and negative charges, respectively. The net effect was electrically negative. However, oxide traps can also be divided into bulk and

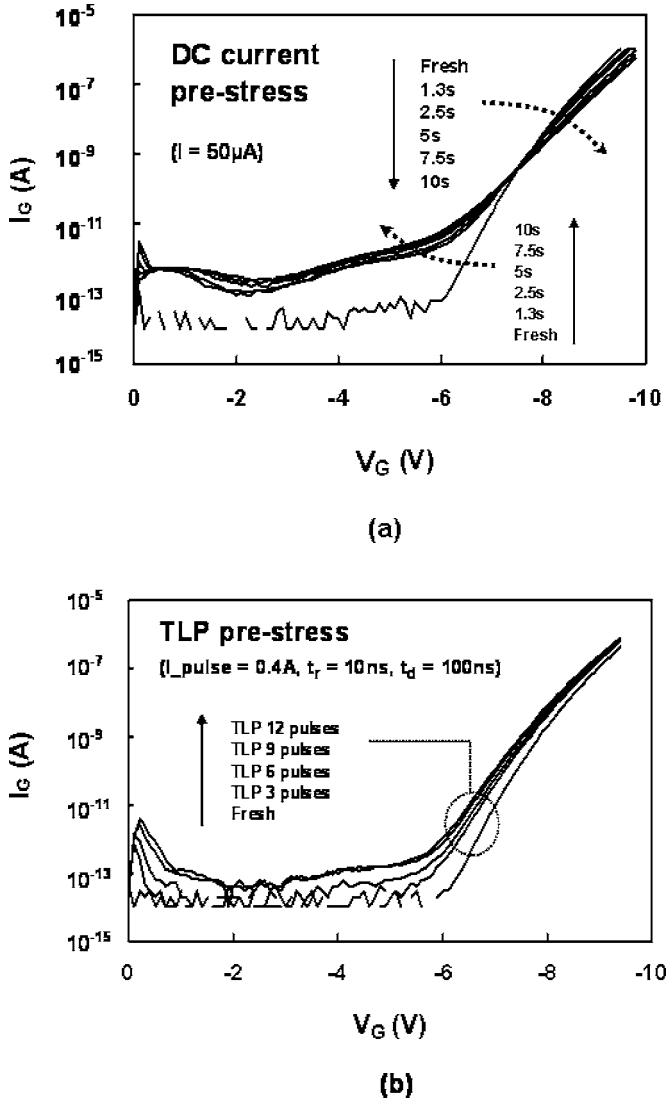

FIG. 4. The *I-V* characteristics of NMOS capacitors subjected to (a) dc constant current and (b) TLP impulse current prestresses. In comparison with dc prestress, the leakage currents induced by TLP prestress rise as the number of stress pulses increases.

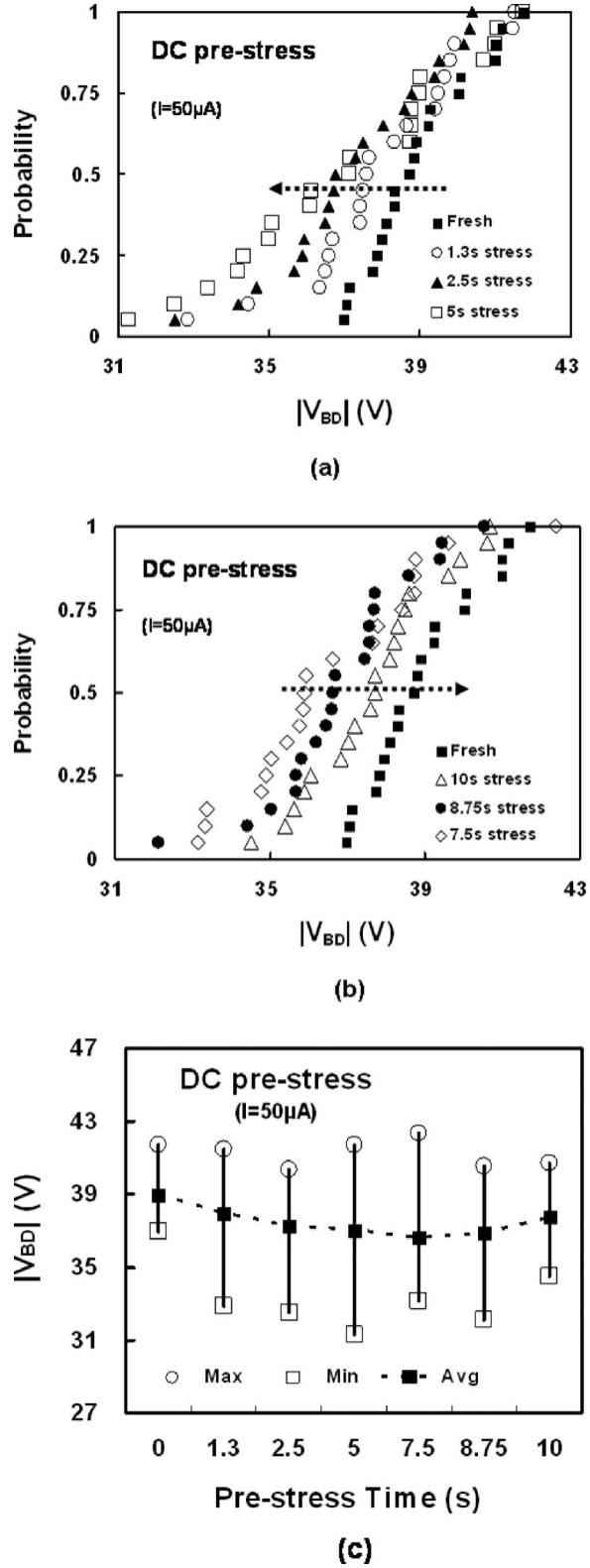

FIG. 5. Typical failure distributions of oxide breakdown voltage for TLP impulse stress on NMOS capacitors, with 50 μA dc current prestress in the ranges of 1.3–5 and 7.5–10 s. The $|V_{bd}|$ vs dc prestress time is shown in (c).

border traps. Border traps lie within a distance of about 3 nm of a Si/SiO_2 interface and can communicate with interface traps and the underlying silicon substrate on time scales of microseconds to seconds.[1] Electrons would have sufficient time to tunnel from interface traps and fill border traps via a trap-to-trap tunneling mechanism at low measurement frequencies.[3] Therefore, these border traps can affect the low frequency characteristics like the interface traps do.

Positive oxide trapped charges generally cause the *C-V* curve to shift to more negative values of gate bias with respect to the ideal *C-V* curve, but negative oxide trapped charges cause the contrary. Interface traps and border traps distort the *C-V* curve when their energy levels cross the Fermi level and change their charges. Figures 3(a) and 3(b) show the quasistatic *C-V* characteristics of NMOS capacitors subjected to dc constant current and TLP impulse current prestresses, respectively. Both stresses clearly exhibit anomalous "humps" and negative flatband shifts. In dc prestress, the positive oxide trapped charges (Q_{ot}^{+}) saturate rapidly, but the number of interface traps (D_{it}) and border traps continues to increase as the stressing time increases. However, the TLP impulse prestress results in increasingly positive oxide trapped charges and interface and border trapped charges at the same time. TLP impulse prestress generated far less in-

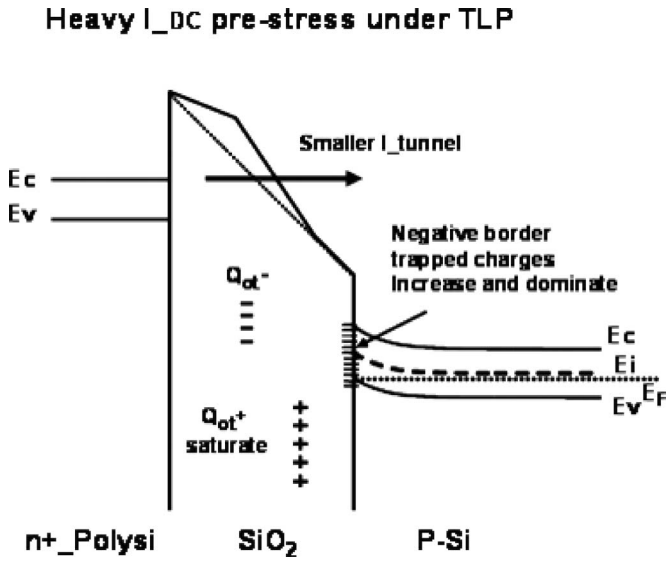

FIG. 6. Schematic diagram of the conduction mechanism under TLP impulse stressing with longer dc constant current prestress time. During the transient TLP biasing, most border traps fail to emit charges and remain negative. The net trapped charges change to negative owing to the successively increasing border traps. Namely, FN tunneling current changes from large to small as the prestress time increases.

terface and border traps than dc prestress did. Note that the fresh devices measured in Figs. 3(a) and 3(b) are different samples on the same wafer but at different locations. A small difference at −0.1 V gate bias can be observed for the different interface and border trap density.

Figures 4(a) and 4(b) show the *I-V* characteristics of NMOS capacitors subjected to dc constant current and TLP impulse current prestresses, respectively. The stress-induced leakage currents by dc prestress rose with increasing prestress time below −8 V gate bias but fell above −8 V gate bias. As reported in previous publications, dc stress-induced leakage current rises by the trap-assisted tunneling completely through the oxide, but drops when negative charges are trapped near the cathode as the electric field further rises.[23,24] By contrast, leakage currents by TLP prestress rise as the stress pulses increase regardless of the applied gate voltage. These findings indicate that TLP impulse prestress leads to increasing positive oxide trapped charges, but dc prestress induces the fast saturated positive oxide trapped charges. The detailed conduction mechanism and schematic energy band diagrams are described later in this study.

B. ESD induced oxide breakdown corresponding to different formations of traps

The TLP curve tracer test system applied square wave forms with 100 ns pulse width and 10 ns rise/fall time to a device to emulate ESD impulse stress. As reported previously, if measurements are performed at a very high frequency, i.e., $f \geqslant 700$ kHz, some interface traps will not be able to follow the ac signal even under strong accumulation.[25] Additionally, the time constants of the border traps are between microseconds and several seconds. Once a transient electric field like a TLP impulse is applied to the gate of the MOS capacitor, most border traps would

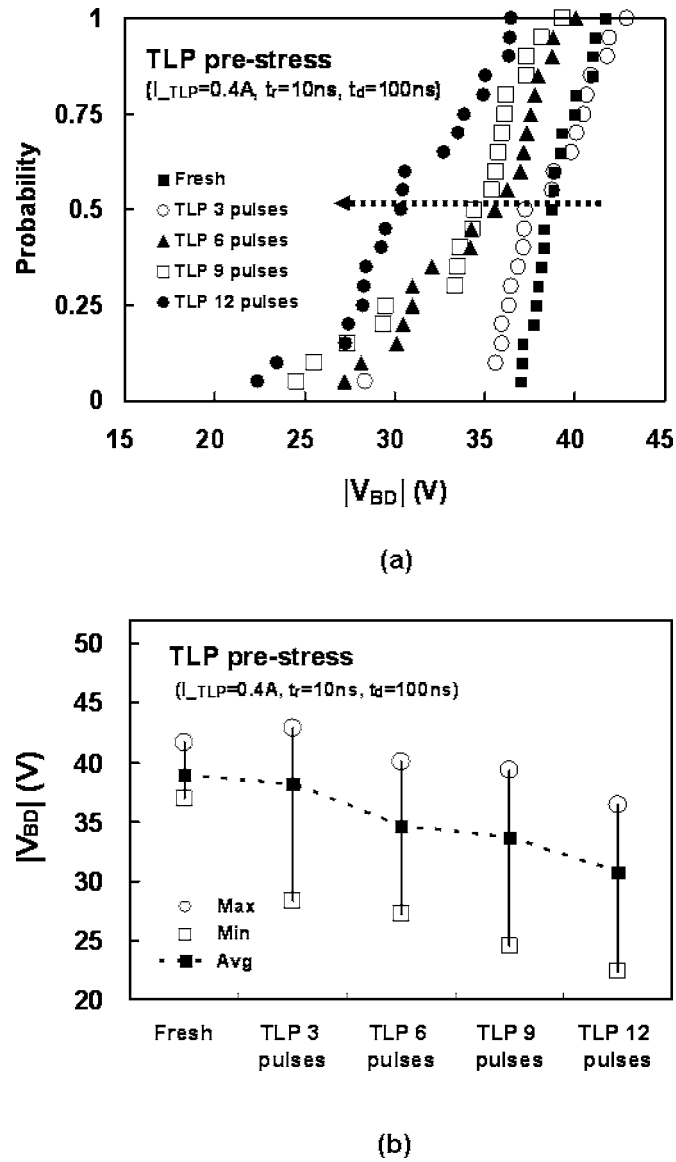

FIG. 7. The typical failure distributions of oxide breakdown voltage for TLP impulse stress on NMOS capacitors with 0.4 A TLP prestress ranging from 3 pulses to 12 pulses. The $|V_{bd}|$ against the number of TLP prestress impulse times is shown in (b).

fail to follow the transient change of electric field to charge or discharge the electrons or holes via the trap-to-trap tunneling mechanism assisted by interface traps. These border traps indeed retain their present electrical polarity under thermal equilibrium condition ($V_G=0$) to reveal electrically negative charges. Therefore, these negative trapped charges would decrease the electric field at the SiO_2/substrate interface during negative TLP impulse stressing, and reduce the Fowler-Nordheim (FN) tunneling current.

Figures 5(a) and 5(b) show the typical failure distributions of oxide breakdown voltage for ESD-like TLP impulse stress on NMOS capacitors with 50 μA dc current prestress in the ranges of 1.3–5 and 7.5–10 s, respectively. Figures 5(c) plots the $|V_{bd}|$ versus dc prestress time. As the figures revealed, a special turnaround phenomenon was observed. Degradations of oxide breakdown voltage initially increased but eventually decreased as the dc prestress time increased.

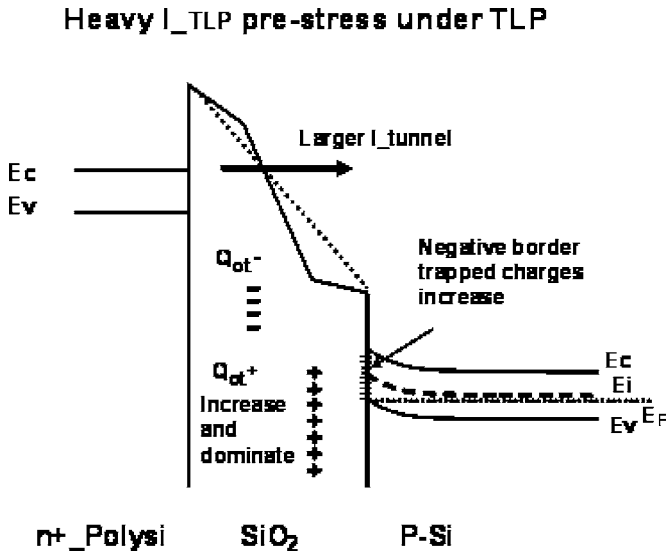

FIG. 8. Schematic diagram of the conduction mechanism under TLP impulse stressing with larger number of TLP impulse prestress times. Applying the TLP bias to the substrate, the larger positive oxide trapped charges dominate over the border traps and cause electric field to increase, therefore resulting in larger FN tunneling current.

Figure 6 shows the schematic energy band diagram of the conduction mechanism under TLP impulse stressing with heavy dc current prestress. Positive oxide trapped charges (Q_{ot}^{+}) appeared to increase the electric field and the FN tunneling current during stressing. However, negative oxide trapped charges (Q_{ot}^{-}) decreased the electric field and the FN tunneling current during stressing. Experimental results indicate that dc prestress generated fast saturated positive trapped charges and increased the number of interface and border traps. Hence, as dc prestress time was lengthened, the numbers of successively increasing border and interface traps would finally dominate over the fast saturated positive oxide trapped charges. Since the border traps reveal electrically negative charges during TLP impulse stressing, the electric field at the SiO_2/substrate interface is therefore high under light dc prestress and low under heavy dc prestress. Simultaneously, FN tunneling current induced by TLP stress also changed from relatively large to relatively small as the dc current prestress time increased. Therefore, a turnaround in the oxide degradation graph was observed.

Figure 7(a) shows the typical failure distributions of oxide breakdown voltage for TLP impulse stress on NMOS capacitors with 0.4 A TLP prestress ranging from 3 pulses to 12 pulses. Figure 7(b) plots the $|V_{bd}|$ against the number of TLP prestress impulse times. These figures indicate that the oxide breakdown voltage decreased as the TLP prestress impulse times increased. Figure 8 illustrates the schematic energy band diagram of the conduction mechanism under TLP impulse stressing with heavy TLP impulse prestress. These test results clearly indicate that more abundant positive trapped charges (Q_{ot}^{+}) dominated over the border trapped charges. In addition, these increasing net positive trapped charges increased the electric field and the FN tunneling current, thus degrading the oxide integrity.

IV. CONCLUSIONS

The trapped charge effect on gate oxide degradation subjected to ESD impulse stressing is studied herein. Different prestress types revealed different trap formations and behaviors. Increasing TLP impulse prestress obviously increases the positive oxide trapped charges and interface and border trapped charges, whereas dc constant current prestress generates fast saturated positive oxide trapped charges as well as successively increasing interface and border traps. Therefore, ESD emulation by TLP reveals a turnaround phenomenon of oxide breakdown characteristics under dc prestress. However, under TLP impulse prestress, the degradation continues to increase as the number of TLP prestress impulses increases. An impulse prestress thus appears to be a highly critical issue for the ESD immunity in devices and products.

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