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Latent damage and parametric drift in electrostatically damaged MOS transistors

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Summary

The relationship between parametric drift and latent damage in ESD gate-stressed MOSFETs is studied. Sub-breakdown damage causes minor characteristic distortion, which may remain undetected until failure. However, such damage is only significant within a narrow stress-voltage window.

Oxide breakdown may cause straightforward malfunction (i.e. *catastrophic failure*) or degraded transistor action. Degraded devices can degenerate further under working voltages (0–10 V), providing a *latent* failure mechanism. Degradation phenomena are attributed to the intrusion of polysilicon gate-material into the oxide and channel regions.

Catastrophically failed and degraded devices are modelled using the *PSpice* circuit simulation system. The effects of degradation upon CMOS logic operation are also examined.

1. Introduction

Electrostatic discharge (or ESD) has long been recognized as a reliability hazard in the semiconductor industry. It may strike wherever devices are exposed to charged bodies, and may cause immediate catastrophic failure or sub-critical '*latent*' damage. Although the former is easily eliminated, the latter presents a more difficult challenge: since the affected devices retain their operational characteristics, they may pass a functional quality inspection, and be shipped to a customer. However, the damage sustained may have seriously damaged their inherent reliability, causing them to fail prematurely during working life.

Since the early 1980s, when ESD-induced latency was first identified [1, 2], a considerable amount of research has been published on the topic. Crockett's experiments on packaged CMOS circuits [3] showed that low-voltage (1 kV) ESD pulses rendered devices more sensitive to high-voltage (2.5 kV) stress. Later work by Aur et al. [4] showed a reduced hot-electron reliability in MOSFETs subjected to ESD pulses.

Sub-catastrophic ESD can also cause variation in component characteristics. Holmes [5], for example, showed that an ESD gate-pulse below the oxide breakdown voltage produced a negative shift in the strong-inversion threshold voltage V_T. This was often sufficient to drive enhancement (E) mode MOSFETs into depletion (D) mode, causing logical malfunctions. Several other workers [6–8] found that ESD gate-pulses moderately higher than the oxide breakdown threshold could distort a MOSFET's I/V characteristic, causing a reduction in the transconductance g_m. Soden and Hawkins [8] found that g_m reduction in CMOS circuits is accompanied by a supply-current increase, introducing a battery-failure hazard in portable equipment. All these phenomena were also predicted by Syrzycki's theoretical model [9].

The present work examines the relationship between latent damage and characteristic variation in MOS transistors. Attempts are made to correlate parametric drift and oxide wearout in MOSFETs subjected to ESD gate-stress. The degradation of walking-wounded devices towards catastrophic failure under working voltage conditions is also studied. Tentative attempts are made to model this degradation using the MicroSim *PSpice* software.

2. Apparatus and test structures

Figure 1 shows the apparatus used in these studies. The devices were tested at wafer-level using a chuck/microprober system. The Hartley 'AutoZap' supplied human-body-model (HBM) ESD pulses, which were applied to the device under test (DUT) between the gate and the wafer substrate contacts. Figure 2(1) shows the equivalent circuit of the AutoZap. The 2-way relay allows the discharge capacitance C_1 to be charged from a Keithley 230 voltage source (accurate to ± 10 mV) to the required pulse voltage V_p, and subsequently discharged into the device-under-test (DUT) via the discharge resistor R_2. Figure 2(2) shows a typical ESD pulse voltage waveform for a 1.5 kΩ resistive load. The effect of ESD upon the DUT's d.c. characteristics was observed using the Hewlett Packard HP4145B parametric analyzer (accurate to ± 1 mV, ± 100 nA). Room temperature (approx. 25°C) and strong illumination were maintained throughout the experiments.

The experimental samples were depletion and enhancement mode NMOS transistor arrays. The structures were fabricated on 3″ diameter wafers of ⟨100⟩ bulk silicon, p-doped to 6.6×10^{14} cm^{-3}. The n^+ source and drain regions were formed by 100 keV arsenic ion-implantation to a density of 2×10^{20} cm^{-3}. Channels were preferentially implant-doped to a net concentration of 4×10^{15} cm^{-3} using boron (p) in the E-mode devices and phosphorus (n) in the

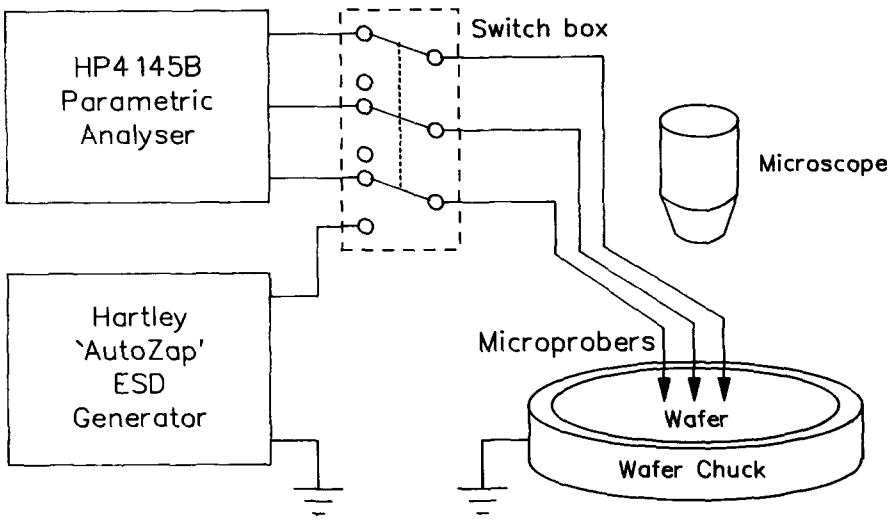


Fig. 1. Block diagram of the experimental apparatus.

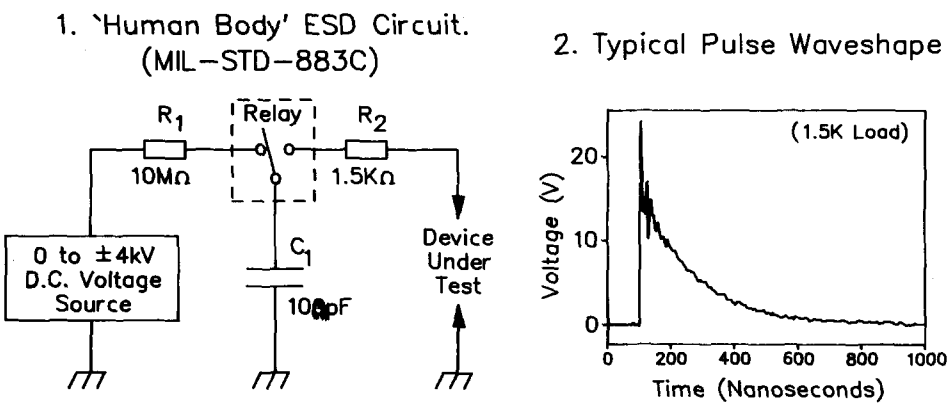
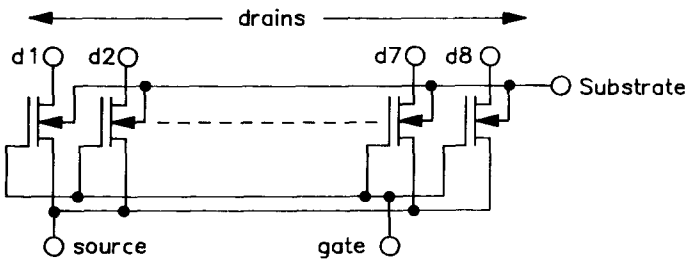


Fig. 2. (1) AutoZap equivalent circuit (MIL-STD-883C human body model specification) and (2) typical output waveform (into 1.5 kΩ resistive load).

D-mode devices. Gate oxides were grown in O_2 under 950°C to a thickness of 40 nm, upon which the 455 nm polysilicon gate electrodes were CVD deposited. The gate polysilicon was As (n^+) doped to a density of 1×10^{21} cm^{-3}. The field-oxide was 0.6 μm thick, and was supplemented by a 1.5 μm Si glass passivation layer.

The transistor structures were fabricated in arrays of eight devices (denoted d1–d8), with common gate and source terminals and individual drains. Since

(a) Circuit Diagram of MOSFET Array Structure



(b) Physical Dimensions of Test Transistors

Type	d1	d2	d3	d4	d5	d6	d7	d8
NMOS(E)	W=25 L=3.5	W=32 L=3.5	W=35 L=3.5	W=42 L=3.5	W=46 L=3.5	W=63 L=3.5	W=40.8 L=3.5	W=102.9 L=3.5
NMOS(D)	W=25 L=3.5	W=32 L=3.5	W=35 L=3.5	W=42 L=3.5	W=46 L=3.5	W=63 L=3.5	W=40.8 L=3.5	W=102.9 L=3.5

(W = channel width, L = channel length, all dimensions in micrometers)

Fig. 3. (a) Interconnection of devices in MOS transistor array, (b) device dimensions.

the ESD pulse charge (C_1 V_p) may not be evenly distributed between the device gates, each array was analyzed as a single unit rather than a set of independent structures. Although this adds an unfortunate complication, it simulates an actual I.C. input in which many gate structures are connected to a single pin. Figure 3 shows a circuit diagram of the interconnections, together with the dimensions of the various structures.

3. Sub-breakdown latency and parametric drift

3.1. Experiment

The initial phase of this study concerned sub-breakdown ESD damage, i.e. latent damage produced by ESD pulses *below* the oxide breakdown voltage threshold V_{bd}. Parametric drift was characterised in terms of the transconductance g_m and the strong-inversion threshold voltage V_T. These parameters were defined as the gradient and intercept of the I_d vs. V_{gs} curve in the saturation region (Fig. 4), with the drain-source potential V_{ds} fixed at +7 V.

The experiments were performed using NMOS E-mode transistor arrays. Each device in each array was characterised in terms of its initial transconductance $g_m(0)$ and initial threshold voltage $V_T(0)$. Negative polarity ESD pulse sequences were applied to the gate structures and g_m and V_T were measured for each device after each pulse. The process was continued until oxide breakdown was observed in terms of a measurable gate current I_{gs}.

The data was then processed in the following manner: The values of g_m and V_T for each device after each pulse were expressed as a percentages of g_m (0)

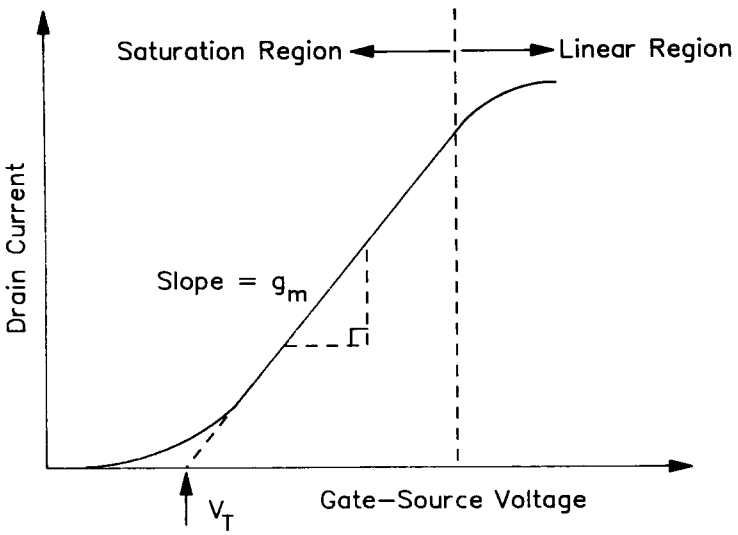


Fig. 4. Extraction of g_m and V_T parameters from MOSFET transfer characteristic.

and $V_T(0)$, yielding the percentage values $g_m(\%)$ and $V_T(\%)$. The average values of $g_m(\%)$ and $V_T(\%)$ for all the devices in the array was plotted against the number of pulses n.

Figure 5 shows the resulting graph for −48.5 V ESD pulses. The error bars indicate the standard mean error, i.e. ±[standard deviation]/√[no. of samples], for each data point. While g_m remains approximately constant prior the breakdown, it suddenly drops after breakdown (in agreement with earlier studies [6–8]). The average value of V_T decreases during the pulse sequence, suggesting the occurrence of positive charge trapping. Although this agrees qualitatively with Holmes' results [5], the variation does not generally exceed 10% and the latent damage may therefore remain undetected until breakdown.

Figure 6 shows the results of an identical experiment performed using −47.5 V ESD pulses. At this lower voltage, the latent damage per pulse is smaller than in the previous experiment and the array withstands a far greater number of pulses prior to breakdown (a further 20 pulses were required to cause failure). As with the −48.5 V experiment, g_m remains approximately constant and negative charge trapping may predominate alternately throughout the pulse sequence. Again, the average shift does not exceed 10% and is too slight to cause functional errors.

The voltage dependence of latent failure was further examined by repeatedly pulsing NMOS array structures and noting the number of pulses n required to cause breakdown. Twenty five arrays were selected and pulsed at −41 V, −42 V, −43 V, −44 V and −45 V, five arrays at each voltage. Figure 7 shows n plotted as a function of the pulse magnitude, each data point representing the mean value obtained from five structures, with the error bars indicating the standard mean error (i.e. ±[standard deviation]/√[no. of samples]). The

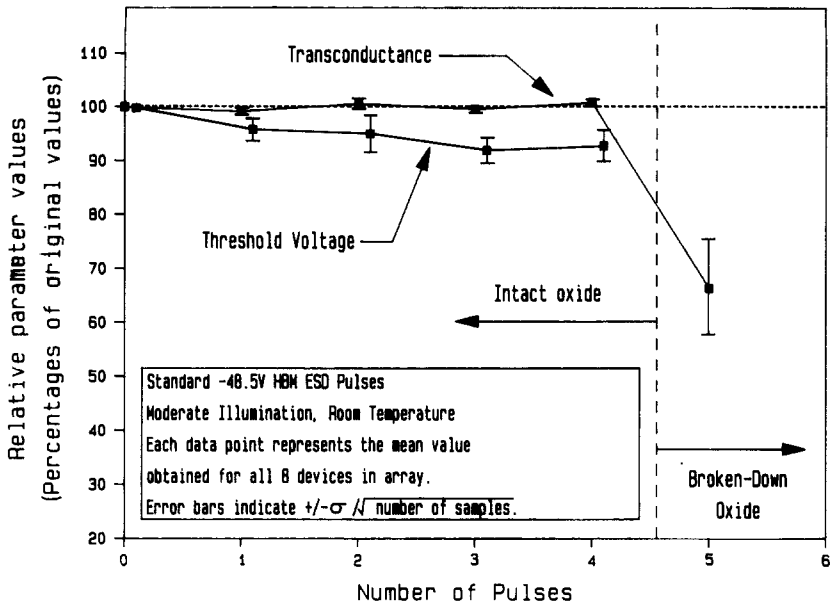


Fig. 5. Sub-breakdown parametric drift in NMOS enhancement transistor array subjected to −48.5 V ESD pulse sequence.

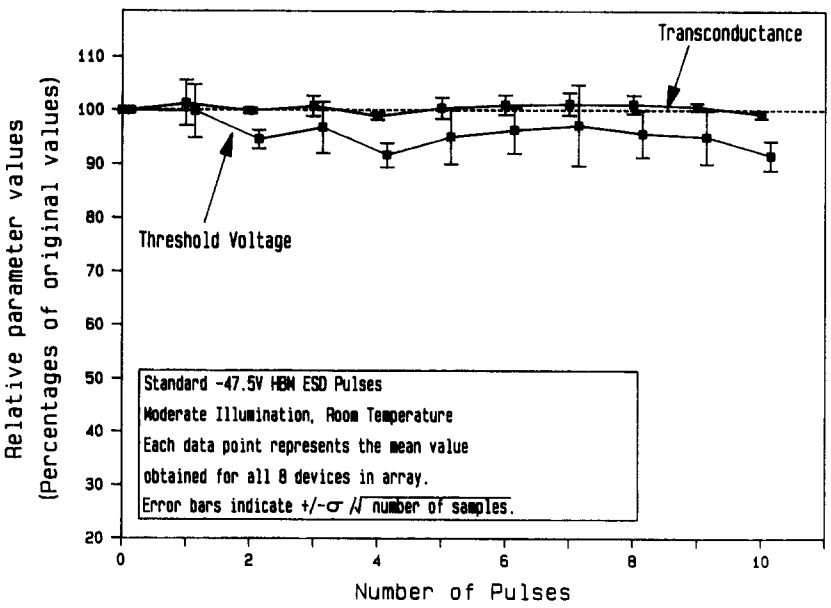


Fig. 6. Sub-breakdown parametric drift in NMOS enhancement transistor array subjected to −47.5 V ESD pulse sequence.

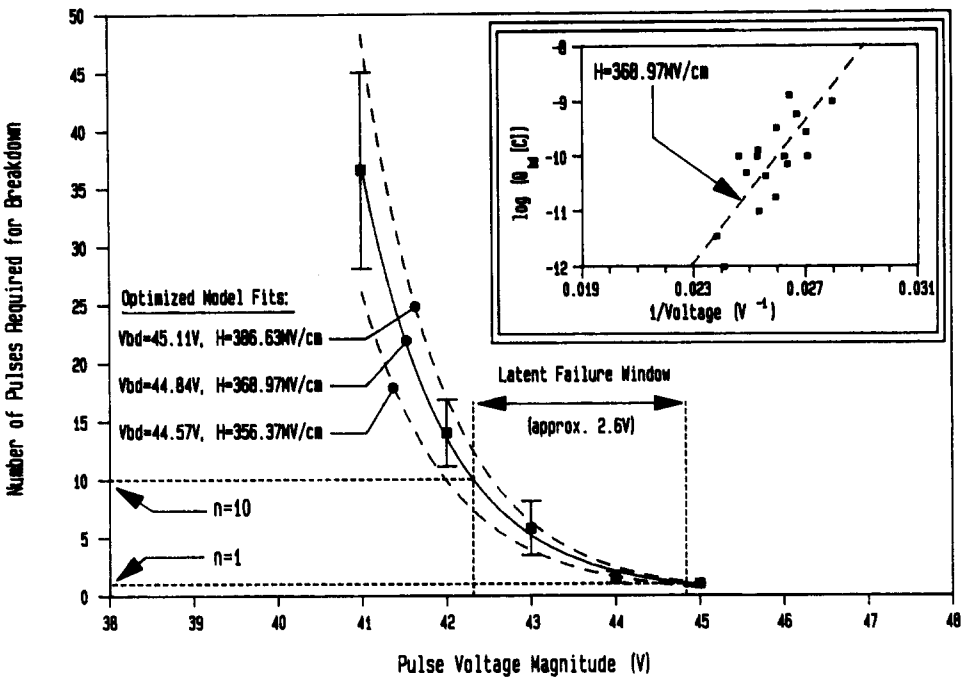


Fig. 7. Number of pulses required for breakdown as a function of pulse voltage. Inset shows log (Q_{bd}) vs. 1/Voltage data reproduced from Ref. [12].

voltage *window* associated with significant latent damage can be conveniently defined as the mean voltage range between the breakdown threshold V_{bd} (where $n=1$) and the voltage at which $n=10$. Figure 7 shows that this window is in the vicinity of 2.6 V, i.e. approximately 5.8% of the breakdown voltage.

Figure 8 illustrates the repeatability of the above experiments. Figure 8(i) shows the coefficient of variation (i.e. standard deviation/mean) associated with each of the data points in Figs. 5 and 6. It is clear that the statistical variation of V_T is generally greater than that of g_m, and can exceed 15% of the mean value. Figure 8(ii) shows a similar analysis of the data in Fig. 7, indicating that inter-device variation of n lies generally between 40 and 100% for $V_p > V_{bd}$ and zero for $V_p > V_{bd}$ (for which n is universally equal to 1).

3.2. Theoretical model

Latent damage can also be modelled using the 'hole-trapping' theory developed by Hu and co-workers [10, 11]. According to this model, electron tunnelling at the oxide cathode supports hole generation and trapping within the dielectric. The subsequent positive space-charge density Q_p (Coul/cm^2)

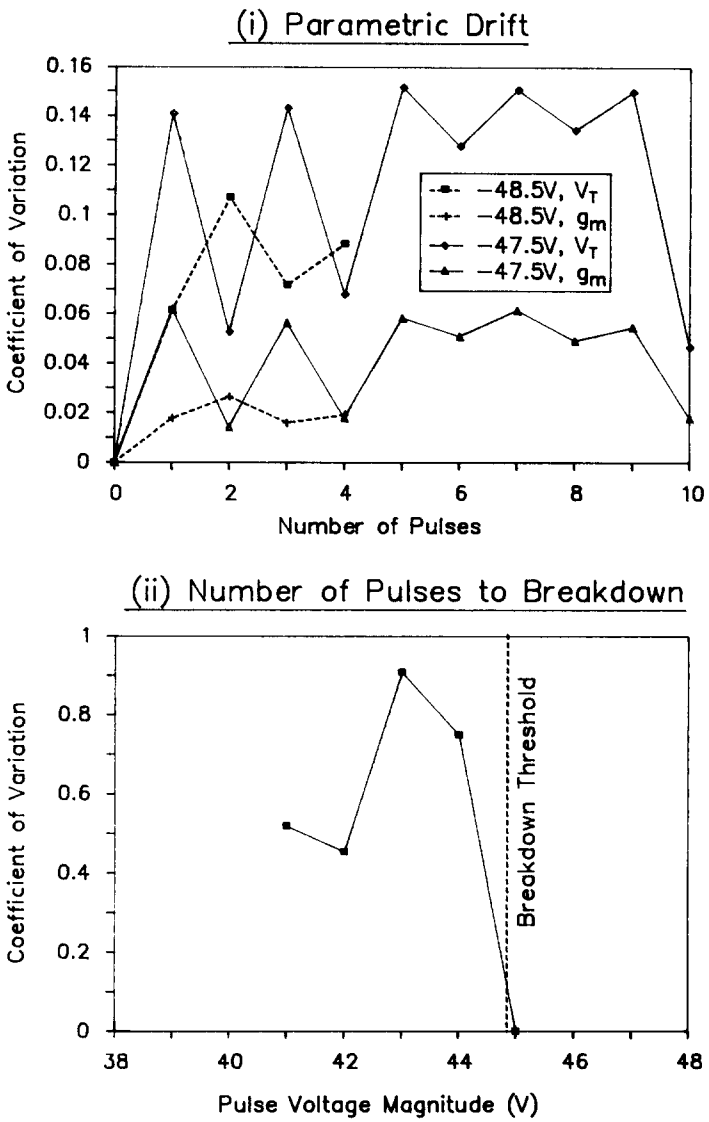


Fig. 8. Coefficients of variation associated with data in Figs. 5, 6 and 7.

may be responsible for the negative V_T drift observed in Section 3. When the Q_p reaches a critical value Q_p^*, the cathode field is noticeably enhanced, increasing in the tunnelling current and causing rapid breakdown. According to the Fowler–Nordheim equation, the tunnelling current I_{ox} is given by

$$I_{ox} = A\,k\,(V_{ox}|T_{ox})^2\,e^{-\frac{BT_{ox}}{V_{ox}}} \simeq A\,J_0\,e^{-\frac{BT_{ox}}{V_{ox}}} \tag{1}$$

where V_{ox} is the oxide voltage, T_{ox} is the oxide thickness, A is the total gate area and k (A/V^2) and B (V/cm) are constants. The parameter J_0 is also approximately constant over a limited field range. The hole generation probability α per injected electron can be modelled by the formula $\alpha = \alpha_0 \, e^{-H/F}$ [10] where F is the oxide field (V_{ox}/T_{ox}) and α_0 and H (V/cm) are constants. Hence in the absence of any de-trapping or trap saturation, the hole charge Q_p may be modelled by the equation

$$Q_p(t) \simeq \frac{\eta}{A} \int_0^t I_{ox}(V_{ox})\,\alpha(V_{ox})\,dt \simeq \eta J_0 \alpha_0 \int_0^t \exp\left(-\frac{(B+H)T_{ox}}{V_{ox}(t)}\right) dt \tag{2}$$

where η is the hole trapping probability. The oxide breakdown criterion is given by $Q_p(t_{bd}) = Q_p^*$, and hence t_{bd} may be predicted for any arbitrary pulse waveshape $V_{ox}(t)$. (This approach was originally pioneered by Fong and Hu [11].)

This model has been extended to predict oxide wearout under ESD stress [12, 13]. During the pulse rise-time, the total pulse charge $C_1 V_p$ re-distributes itself across the entire system capacitance C, reducing the effective pulse magnitude by a factor $L = C_1/C$. The capacitor C then proceeds to discharge into the oxide in accordance with the differential equation:

$$C \cdot \frac{dV_{ox}}{dt} = -I_{ox}(V_{ox}) \tag{3}$$

The oxide voltage profile $V_{ox}(t)$ may be obtained analytically from eqn. (3) (using the boundary condition $V_{ox}(t) = LV_p$) and inserted into eqn. (2). An expression for the total trapped hole charge per pulse may then be obtained by performing the integration between $t = 0$ and $t = \infty$, yielding:

$$Q_p^{pulse}(V_p) = \frac{CT_{ox}\eta J_0 \alpha_0}{\tau_0 AkH} \exp\left(-\frac{HT_{ox}}{LV_p}\right) \tag{4}$$

Hence the number of pulses $n(V_p)$ required to support breakdown is equal to $Q_p^*/Q_p^{pulse}(V_p)$, and is given by the expression:

$$n(V_0) = \exp\left(\frac{HT_{ox}}{L}\left[\frac{1}{V_p} - \frac{1}{V_{bd}}\right]\right) \tag{5}$$

where V_{bd} is the breakdown potential (i.e. the value of V_p for which $n = 1$).

Equation (5) was fitted to the experimental data of Fig. 7. The value of $L(= C_1/C = 0.853)$ was independently measured, while V_{bd} and H were determined from the slope and intercept of the log(n) vs. $1/V_p$ curve. This process

was performed using the mean values of n and the upper and lower limits of the error bars. The resulting model curves are superimposed on Fig. 7, together with the corresponding parameter values. It is noticeable that the majority of the variation between the upper and lower curves appears in the parameter H (8.2%), while a mere 1.2% variation exists in V_{bd}.

The plausibility of the model was checked by means of the constant-voltage charge-to-breakdown Q_{bd} data reproduced from Ref. [12] (see inset on Fig. 7). This data was obtained using structures identical to those used in this paper. Re-arrangement of eqn. (2) shows that the log (Q_{bd}) vs. 1/Voltage curve should have a slope equal to $HT_{ox}\log(e)$. The inset on Fig. 7 shows that such a slope calculated from the central value of H (368.97MV/cm) is indeed compatible with this data.

4. Latent damage and parametric drift in damaged-oxide devices

4.1. Experimental procedure

Results are reported for 64 NMOS transistors, of which 32 were E-mode and 32 were D-Mode. The devices, all of which conformed to their nominal specifications, had received no prior stress. The procedure was as follows: the devices were initially characterised in terms of their I_d vs. V_{ds} and characteristics and were then subjected to single ESD pulses of -200 V, -100 V, $+100$ V, and $+200$ V. One specimen of each array type was stressed at each voltage. The I_d vs. V_{ds} curves were then re-measured and compared with the original characteristics.

Since many of the devices were in a delicate latently-damaged condition immediately after pulsing, a characterisation method was required which subjected them to minimum measurement stress. The magnitudes of V_{ds} and V_{gs} were therefore kept within ± 1 V during characterisation. Figure 9 shows typical characteristics of undamaged devices.

The characteristics of some of the degraded devices were then re-measured using V_{ds} and V_{gs} ranges of 0–10 V, in order to examine the effects of working-voltage stress upon the characteristics. Since V_{gs} is common to all the devices in an array, only one device per array was subjected to such measurement.

4.2. Results

The post-ESD characteristics were classified into the following categories:

Group 1. Unchanged characteristics.
Group 2. Characteristics with negatively-shifted V_T.
Group 3. Characteristics with reduced g_m, converging at origin.
Group 4. Characteristics with reduced g_m not converging at origin.
Group 5. Linear resistive characteristics.
Group 6. Characteristics with zero g_m.

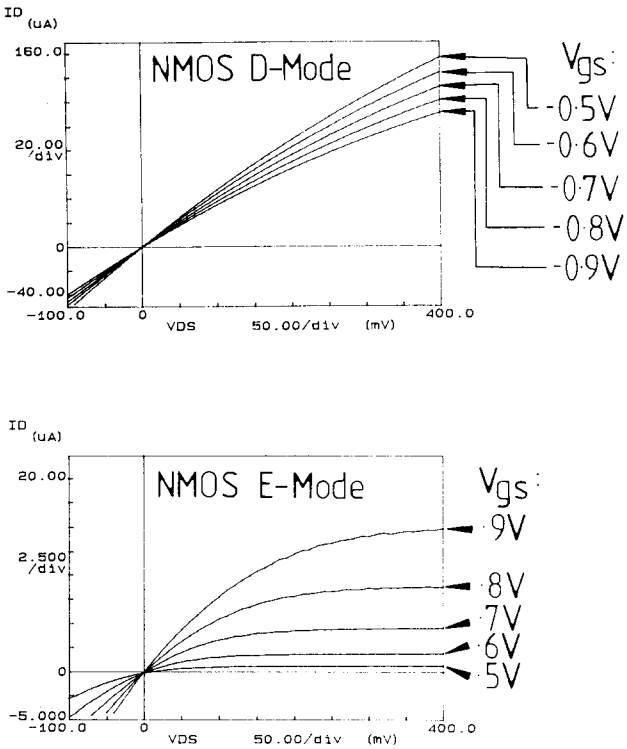


Fig. 9. Typical I_d vs. V_{ds} curves for undamaged NMOS transistors.

Typical characteristics from each category are shown in Fig. 10. Groups 2–4 clearly belong to the 'degraded characteristic' category, while Groups 5 and 6 are catastrophic failures. The threshold-voltage variation in Group 2 was sometimes of the order of several volts, causing E-mode devices to effectively become D-mode. The transconductance reduction in Groups 3 and 4 varied between about 5% and 95% (anything beyond a 95% reduction was classed as a Group 6 failure). Figure 11 shows which of the devices on each array fell into each category.

Many of the devices whose characteristics were re-measured using $0 < V_{ds} < 10$ V maintained stable characteristics. Others, however, underwent further degradation during characterisation. Figure 12 shows the characteristics of two walking-wounded devices (originally of Groups 2 and 4) after they had received three characterisations. (A typical undamaged device characteristic is shown for comparison.) These devices are clearly unstable under working voltage stress and therefore constitute a latent hazard.

Further experiments were performed in order to observe this degradation phenomenon in action. Figure 13 shows the transfer characteristics (I_d vs. V_{gs}) for an NMOS E-Mode device during the degradation cycle. Characteristics

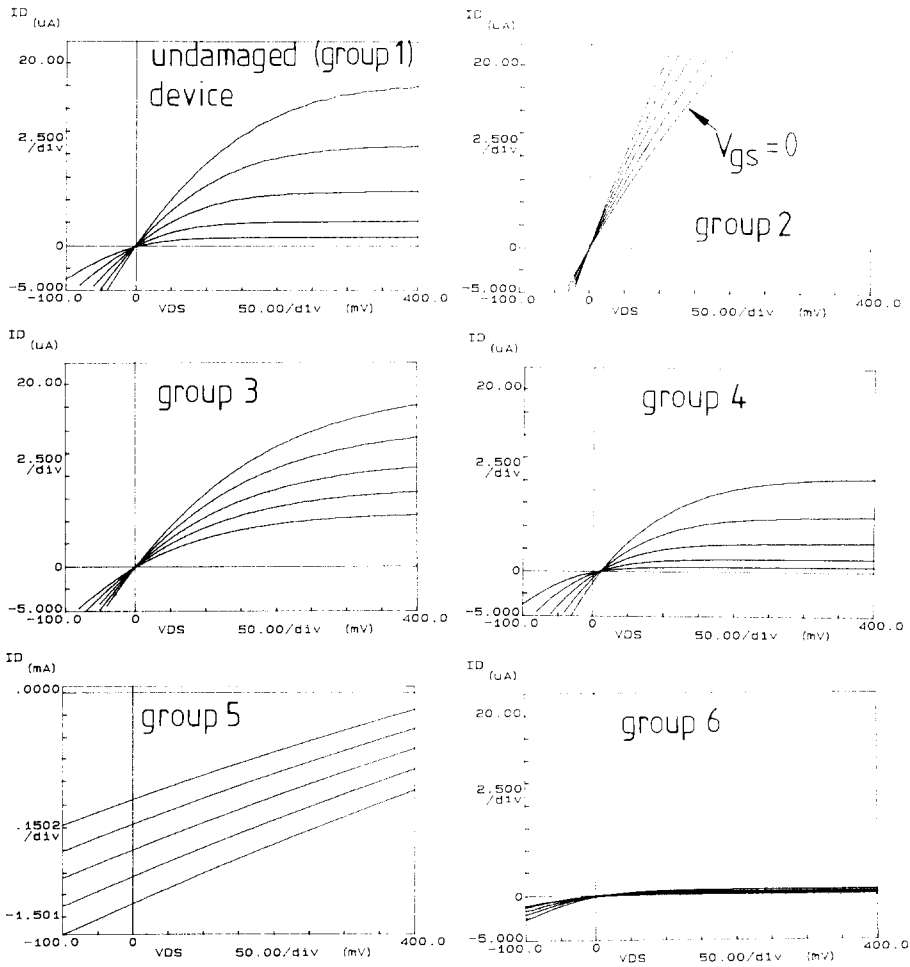


Fig. 10. Post-breakdown characteristics of NMOS E-Mode transistors.

A and B were measured immediately before and after the application of a −80 V ESD pulse, while characteristics C and D show the results of subsequent characterisations. Since characteristics B and C possess positive transconductances ($\partial I_d / \partial V_{ds}$), they must be classified as non-catastrophic degradation states. However, characteristic D is clearly a catastrophic failure of Group 5 (see Fig. 10). Degradation is displayed by the spasmodic jumps of characteristics B and C, which cause the device to drift towards catastrophic failure under working-voltage stress.

In a limited number of cases, repeated characteristic re-measurement caused an eventual return to transistor action. In this recovered state, the transistors were extremely robust and could often withstand ESD pulses up to several

NMOS D-Mode Transistors

Voltage	d1	d2	d3	d4	d5	d6	d7	d8
-200V	1	1	1	1	1	2	2	2
-100V	3	3	1	1	1	1	1	1
+100V	2	2	2	2	2	5	2	2
+200V	2	2	2	2	2	2	2	5

NMOS E-Mode Transistors

Voltage	d1	d2	d3	d4	d5	d6	d7	d8
-200V	6	6	6	6	6	6	4	4
-100V	6	6	6	3	3	3	3	1
+100V	3	5	2	3	3	3	3	5
+200V	2	2	2	2	2	2	5	2

Fig. 11. Distribution of Categories 1 to 5 in NMOS arrays.

hundred volts. However, these cases were rare, and most catastrophically failed devices retained in their characteristics indefinitely.

4.3. Discussion and modelling

Dielectric breakdown in MOS oxides is believed to be accompanied by the intrusion of one or more filaments of polysilicon gate material into the SiO_2 [8]. These filaments can form conductive paths between the source, drain and gate terminals, or between the gate electrode and the channel. The geometry and position of the filaments dictate the nature of the failure characteristics [9].

4.3.1. Qualitative analysis of failure characteristics

Group 2 characteristics are clearly extreme cases of the negative V_T drift encountered in Section 3. In these cases the positive-charge trapping was sufficient to drive E-mode devices into D-mode (or D-mode devices even further into depletion).

Group 3 failures probably result from filaments connecting the gate to the source terminal. Since the filament resistance R_f forms a potential divider with the parasitic gate resistance R_g, the effective gate-source voltage is reduced by a factor $R_f/(R_f+R_g)$, thereby reducing the effective transconductance by the same factor. The characteristic is uniformly scaled-down by the process and the characteristics continue to converge at the origin.

Group 4 failures are caused by gate/drain and gate/channel filaments. When V_{gs} is high and V_{ds} is low, current flows in through the gate and out through the

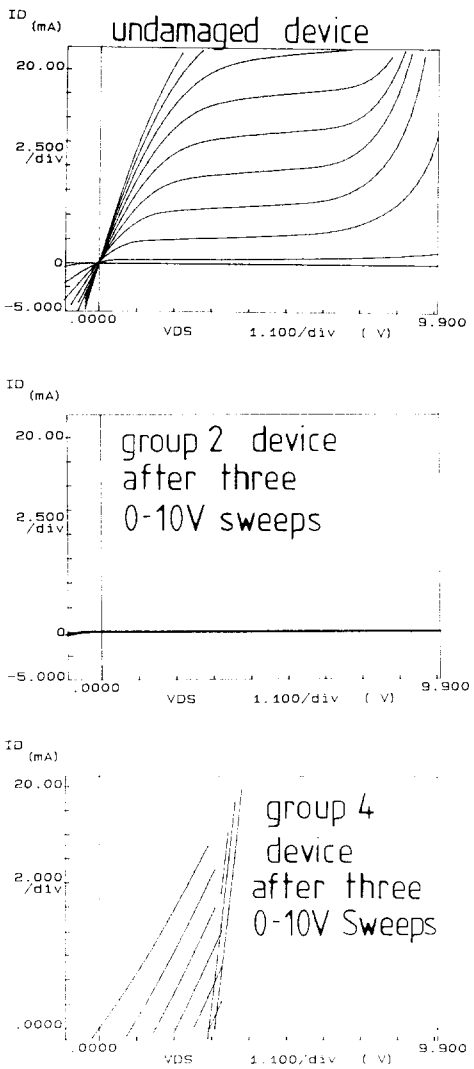


Fig. 12. Characteristics of ESD-degraded transistors (originally of groups 2 and 4) after three 0–10 V characterization sweeps. An undamaged characteristic is shown for comparison.

source, creating a negative I_d for positive V_{ds}. Hence the characteristics fail to converge at the origin. The g_m reduction is caused by inversion-layer charge being sucked out of the channel region into the gate via the damaged oxide.

Group 5 represents an extreme case of the gate-drain breakdown, when the current in the filament resistance R_f dominates the transistor drain current. Similarly Group 6 represents an extreme case of gate-channel breakdown, where practically all inversion charge is depleted via R_f.

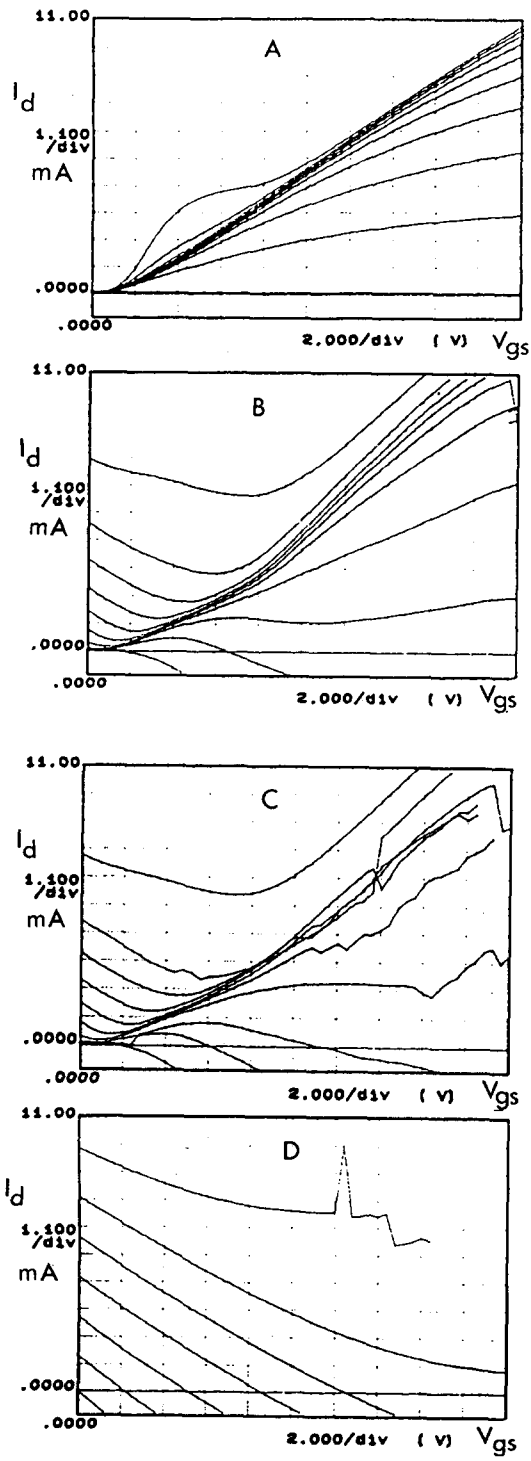


Fig. 13. Characteristics during degradation.

The spasmodic nature of characteristic shifts in Fig. 13 suggests thermal expansion of defects due to joule heating. As the power dissipation in a defect increases during a voltage sweep, the temperature increases quasi-statically until a critical temperature is reached. At this point the defect expands rapidly, reducing R_f, until a new equilibrium is reached. Since this transition is fast for the parametric analyzer to measure, the characteristics appear to consist of discrete curves, punctuated by discontinuities.

4.3.2. PSpice model of failed device

A lumped-element model of a failed transistor was developed using the MicroSim *PSpice* software. The modelling technique (which was based upon that of Syrzycki [9]) assumes that there is no transverse current flow exists within the transistor channel. The basic circuit model is illustrated in Fig. 14. The breakdown filament resistance R_f has three alternative locations: (i) gate-to-source [Group 3 degradation], (ii) gate-to-drain [Groups 4 and 5] and (iii) gate-to-channel [Groups 4 and 6]. Since gate-channel breakdown is accompanied by solid-state diffusion of the n^+ gate dopant into the channel region [9], a rectangular equipotential of dimensions $L_d \times W_d$, was placed within the channel, dividing the structure into three different transistors. The PSpice LEVEL 1 MOSFET model (Shichman-Hodges) was selected, together with

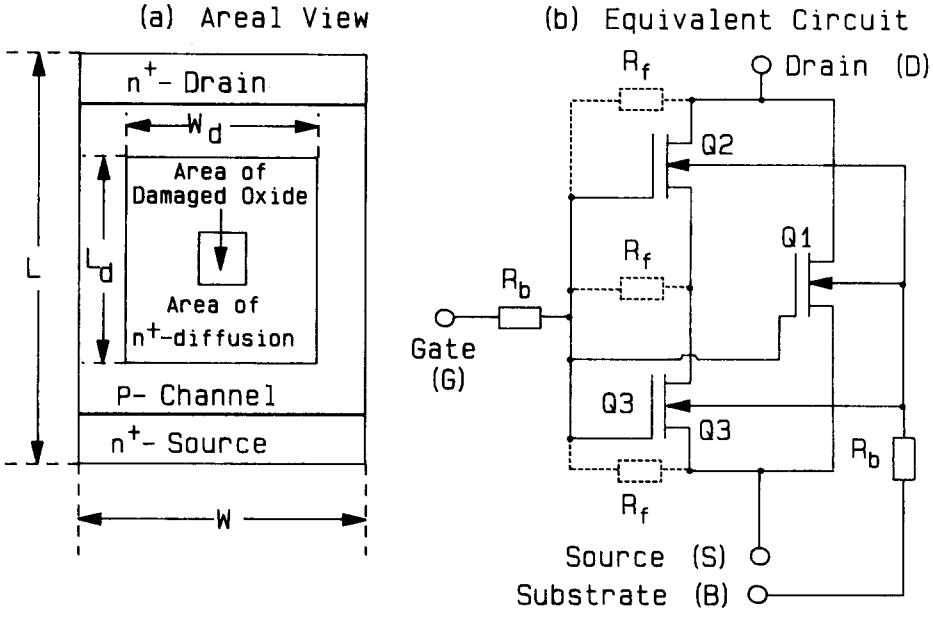


Fig. 14. Schematic areal view and equivalent circuit of damaged MOSFET. The transistor Q1 has length L and width $W-W_d$. The transistors Q2 and Q3 have length $(L-L_d)/2$ and width W_d.

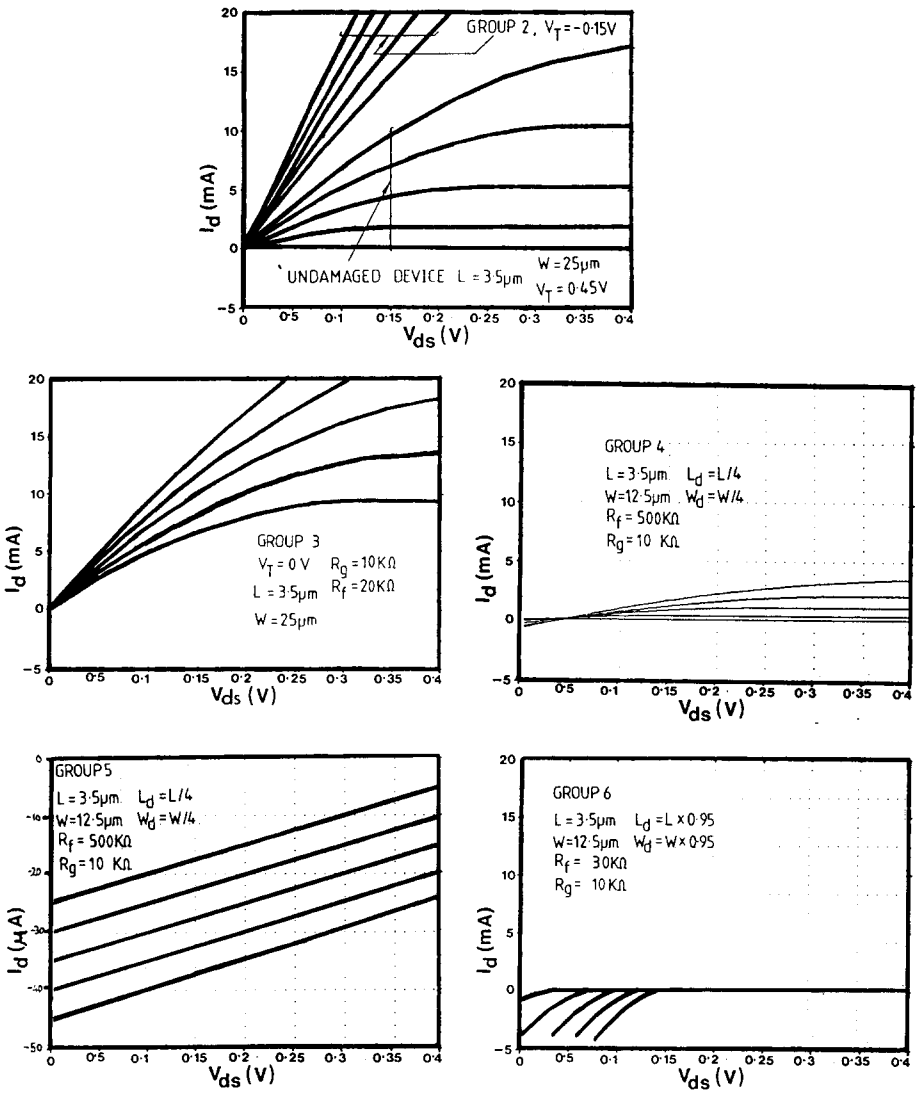


Fig. 15. Failure characteristics predicted using the *PSpice* model.

V_T=0. (Although it assumes constant mobility, it easily applicable to the failure characteristics of Figs. 9 and 10, in which the fields are insufficient to cause mobility modulation.) Figure 15 shows failure the characteristics simulated using this model.

4.3.3. Effect of degradation on CMOS operation

The impact of device degradation upon logic operation is a complex subject which shall be dealt with more fully in a later publication. The present

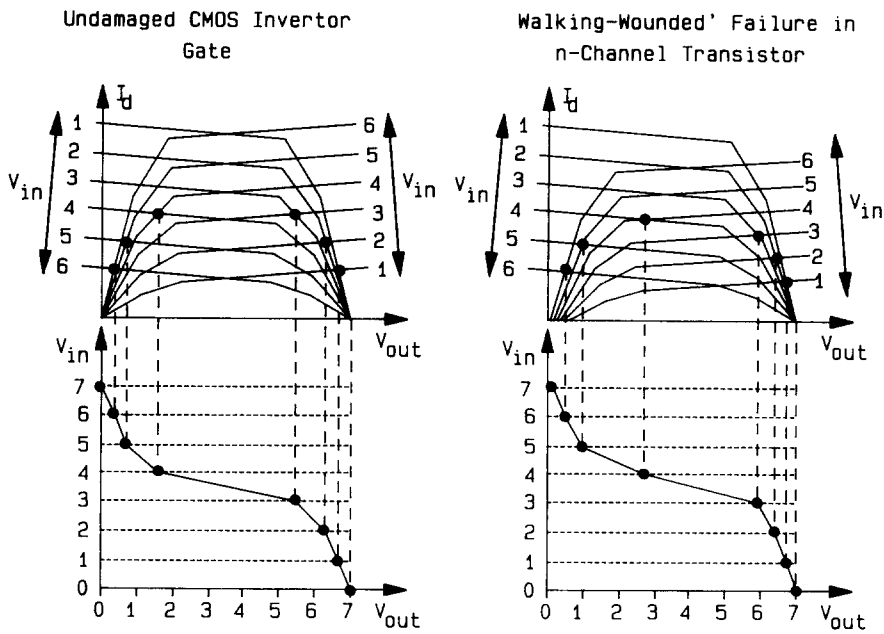


Fig. 16. Schematic representation of the transfer characteristics of a healthy CMOS invertor (left) and a CMOS invertor with a Group 4 degraded n-channel transistor (right).

discussion is confined to the simple CMOS invertor (NOT) gate. The left portion of Fig. 16 shows a graphical representation of the operation of such a circuit. The two transistor characteristics are superimposed and the operating points for a selection of input voltages are transferred to an input vs. output graph. The output clearly exhibits a logical 1 while the input is held at 0 and vice versa.

The right portion of Fig. 16 shows the impact of a degraded (group 4) n-channel transistor on the gate operation. Although the output voltage is positively shifted, the logical inversion function is maintained, illustrating how walking-wounded failure is not necessarily detectable in terms of logic performance [8]. However, continued g_m degradation causes the curve to shift steadily to the right until the circuit enters a 'stuck-at-1' condition.

Figure 17 illustrates the effects of linear catastrophic failure (Group 5) on a CMOS invertor. This type of failure clearly introduces a voltage-follower behaviour, irrespective of which device (n-channel or p-channel) has failed.

5. Conclusions

The relationships between latent damage and d.c. parametric drift in ESD damaged MOSFETs have been studied both experimentally and theoretically.

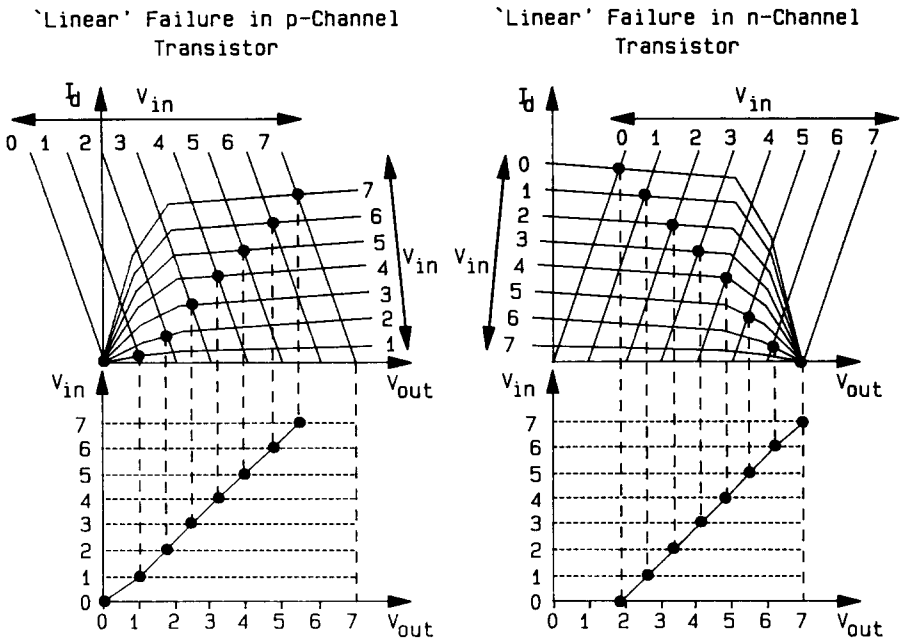


Fig. 17. Schematic representation of the transfer characteristics of a CMOS invertor with Group 5 linear failure in the p-channel transistor (left) and a CMOS invertor with a Group 5 in the n-channel transistor.

The following conclusions can be drawn from the results:

1. Although sub-breakdown latency is difficult to detect in terms of d.c. parametric drift, the extreme narrowness of the latent failure window (determined by theory and experiment) suggests that it is unlikely to be a major reliability hazard. Devices subjected to random-magnitude ESD are most likely to receive pulses greater than V_{bd}, causing immediate failure, or below V_{bd}-ΔV_{lat}, leaving them virtually undamaged.
2. MOS devices with damaged oxides were found to exhibit either walking-wounded or catastrophic-failure characteristics. The former were shown to degrade into the latter under working-voltage stress, providing a latent failure mechanism. The 'jumpy' nature of the characteristic degradation suggested spasmodic defect expansion under Joule heating.
3. The Syrzycki methodology [8] was employed in order to model the transistors at their various stages of degradation. The effect of degradation on CMOS operation was also examined.

However, the reported experimental data is not sufficient to provide a complete picture of the degradation processes. This work merely demonstrates that damaged devices *do* degrade under working-voltage stress and suggests some explanations of this phenomenon. It also provides a springboard for a deeper study which is currently in progress.

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